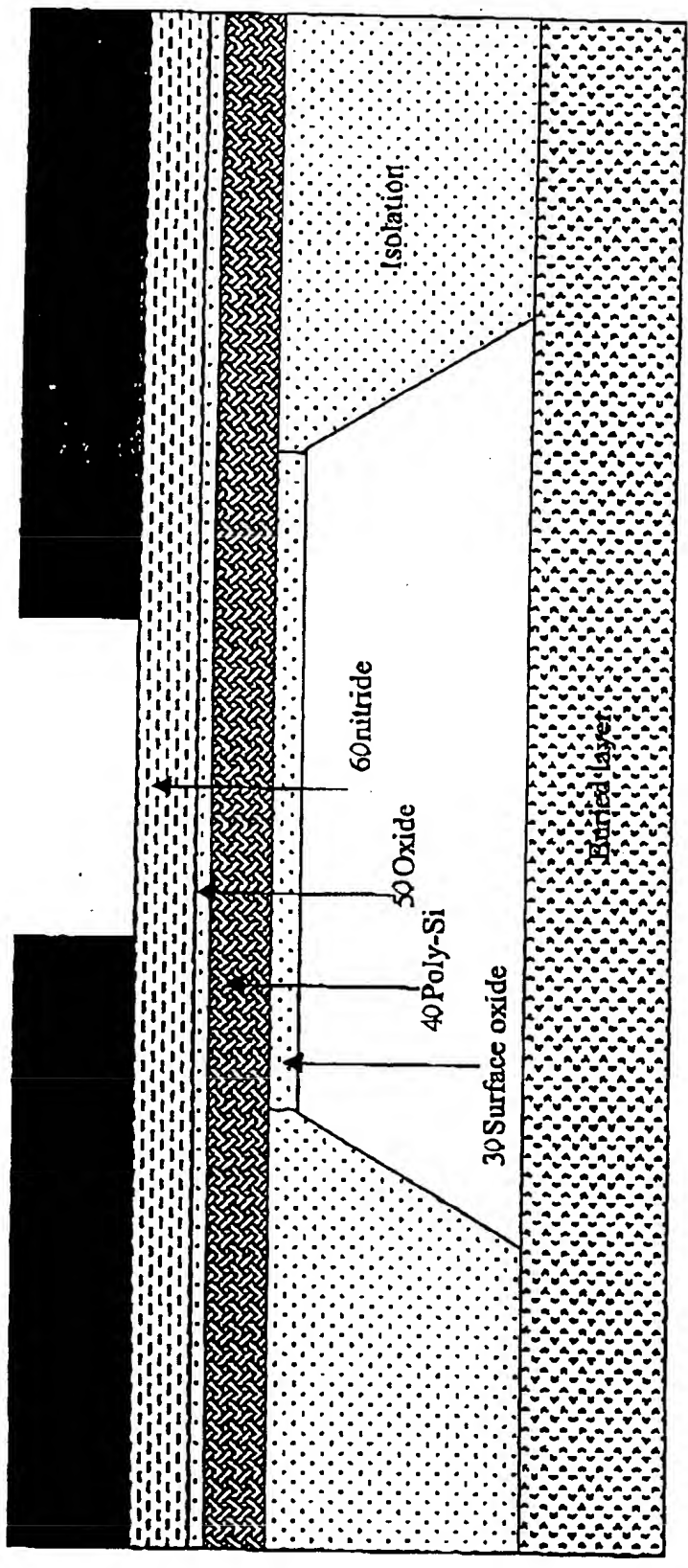


Process:

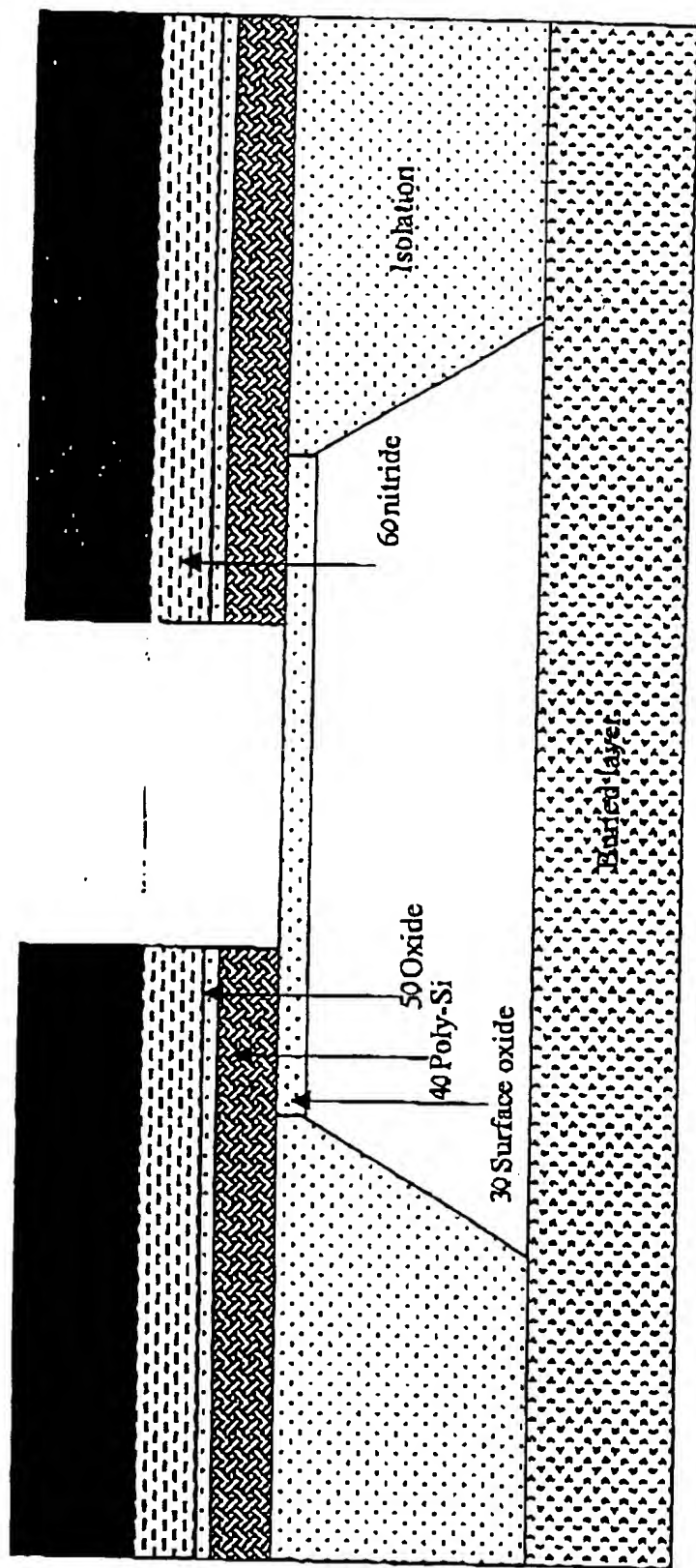
1. Buried layer formation
2. Isolation (STI shown) and collector contact diffusion (not shown)
3. Surface oxidation
4. Poly-Si deposition, thickness \sim equal to the thickness of SiGe base
5. Oxide
6. Nitride

Fig. 1A



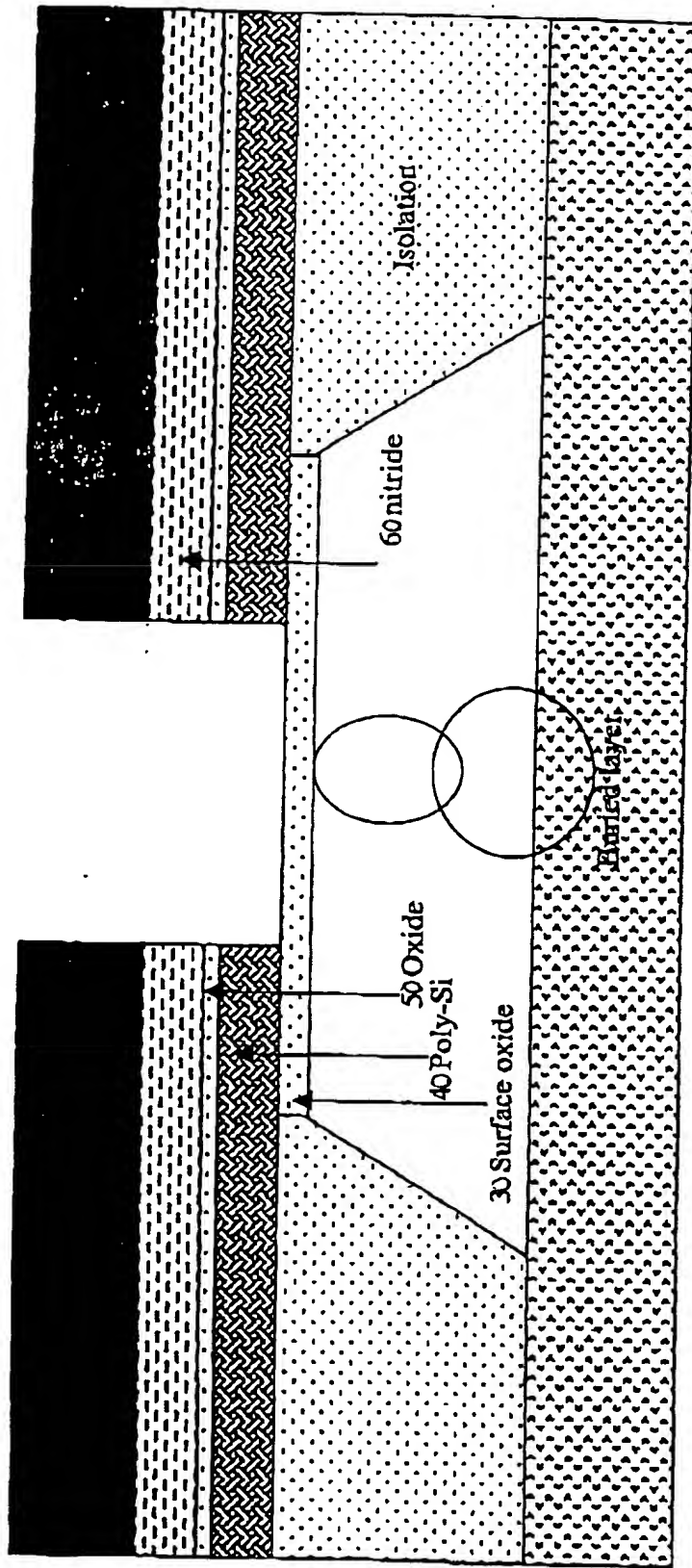
Process:
7. Emitter window mask

Fig. 1B



- Process:
8. Etch nitride, stop on oxide
 9. Etch oxide, stop on poly
 10. Etch poly, stop on oxide

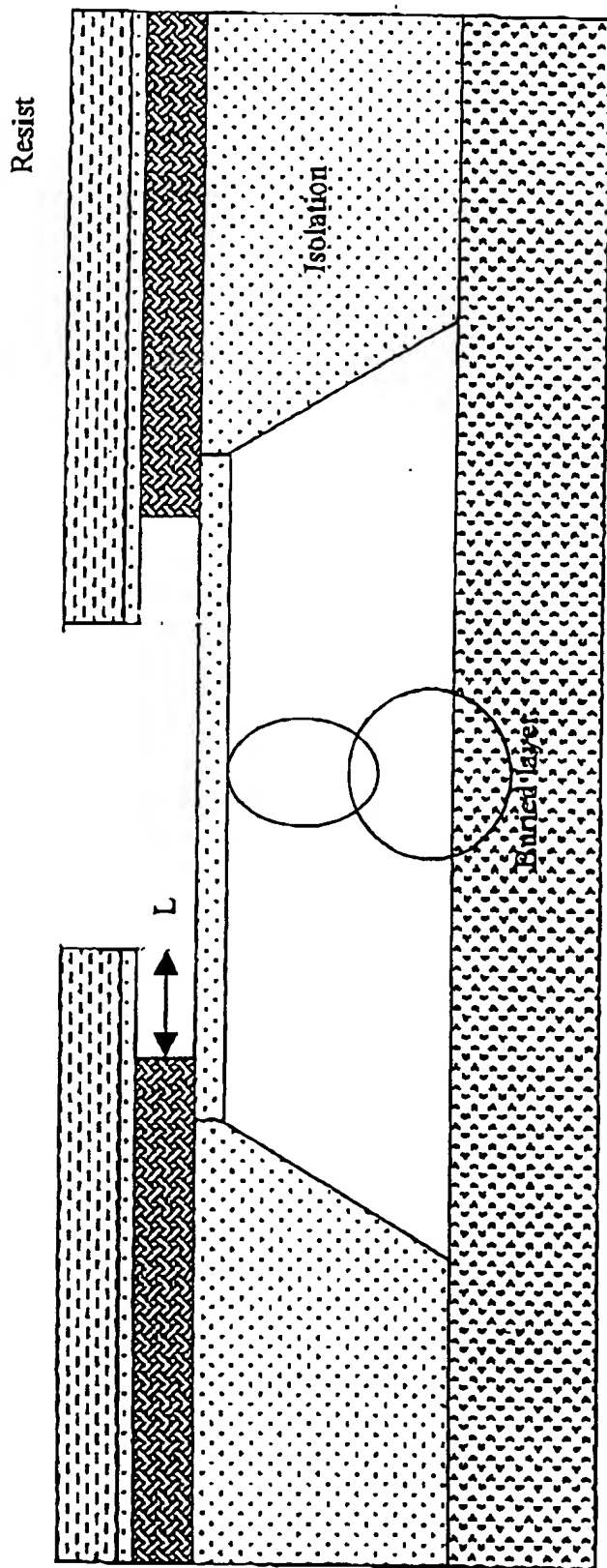
Fig 1C



Process:

11. Implant collector, self aligned to the emitter window opening

Fig 1D



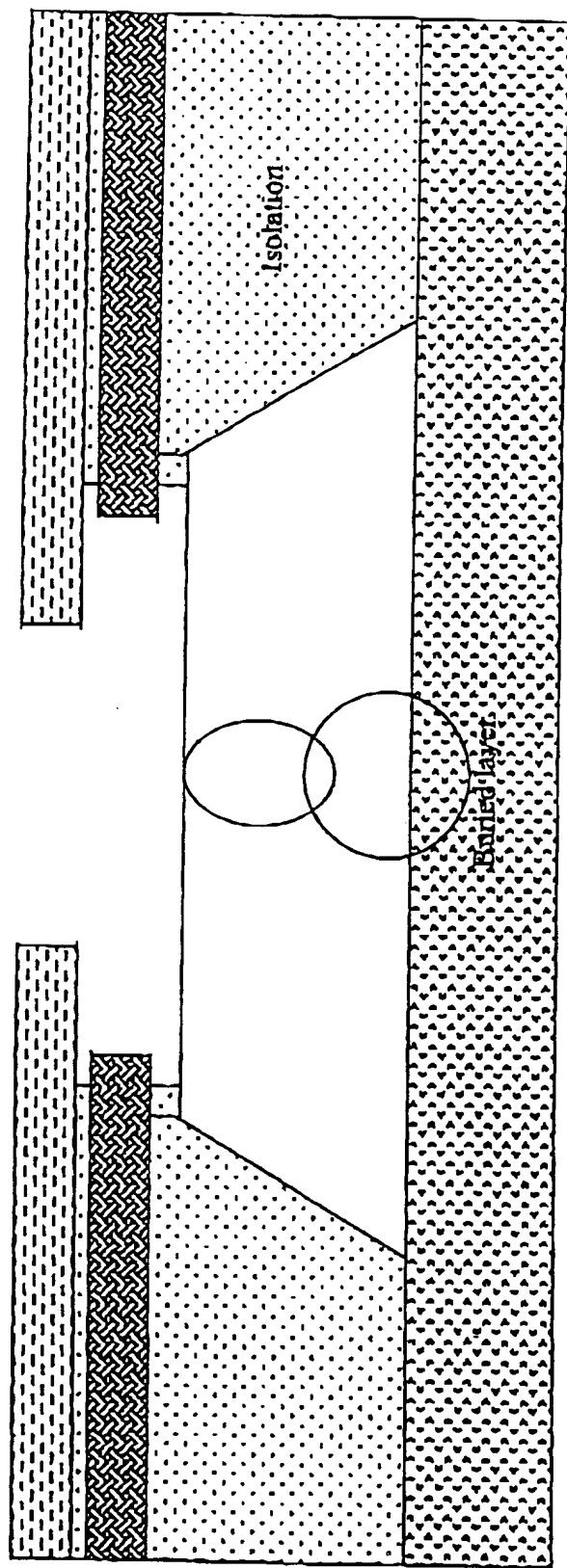
Process:

12. Etch poly-Si laterally, selective to oxide and nitride. L should be greater than poly thickness

- Wet etch, e.g. Choline, carried out after the resist strip

- Dry isotropic etch carried out prior to resist strip, followed by resist removal

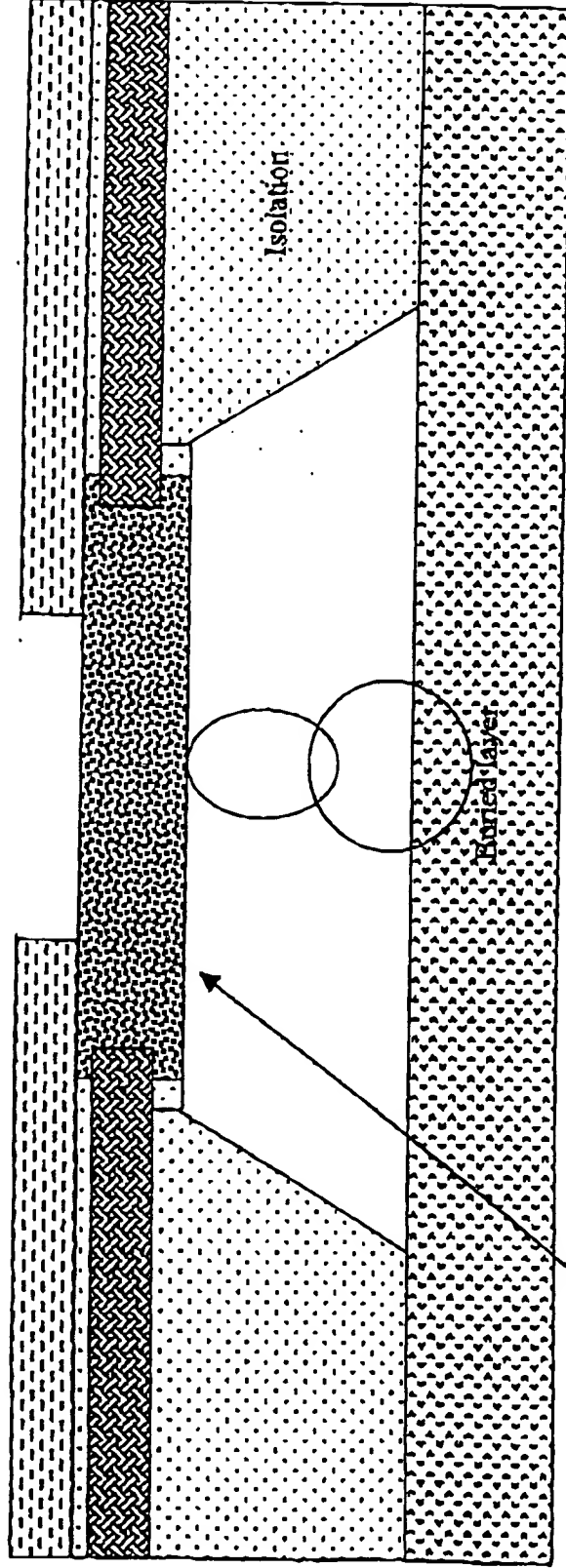
Fig. 1E



Process:

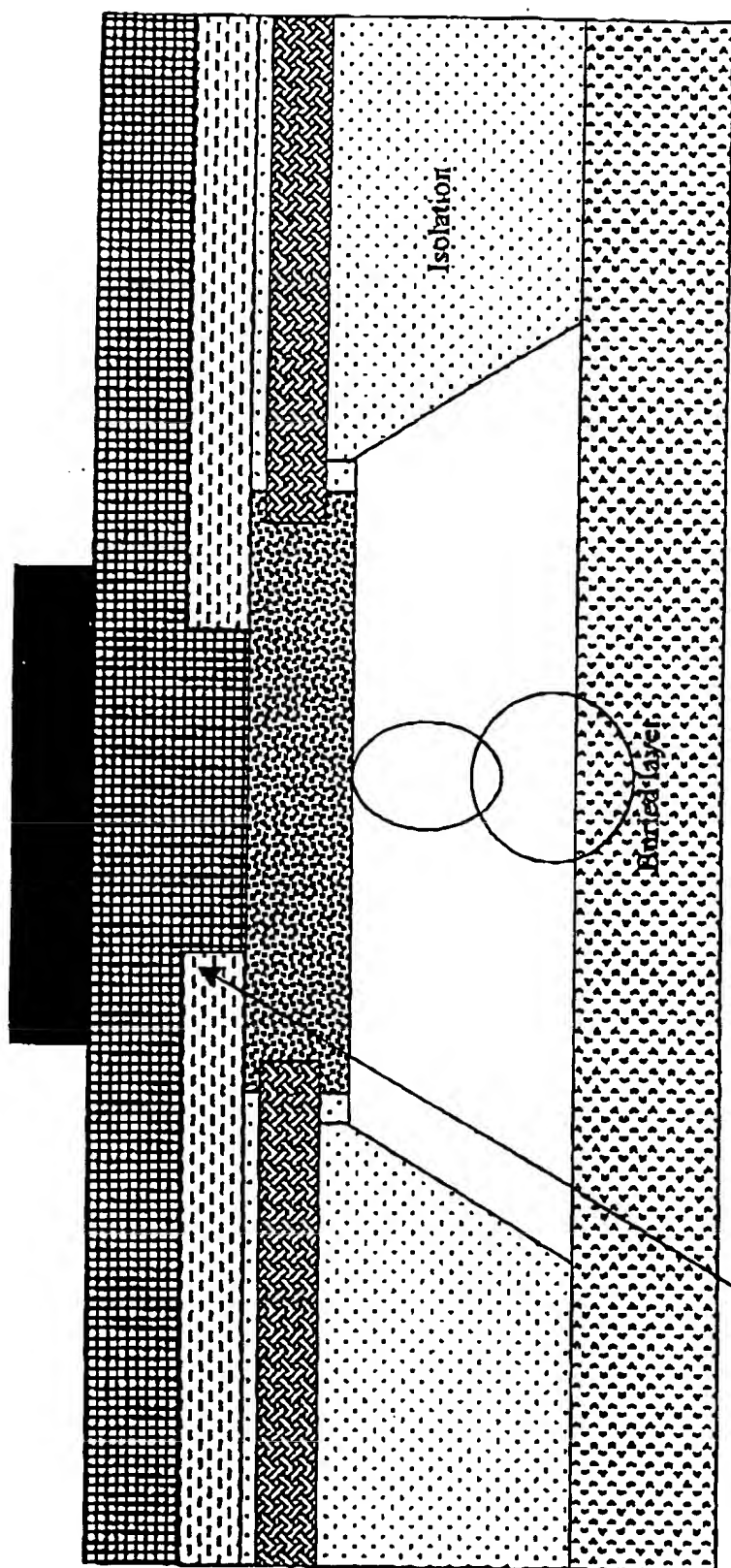
13. Wet etch oxide, prepare surface for selective SiGe deposition

Fig 1F



Process:
14. Selective SiGe deposition

Fig. 16



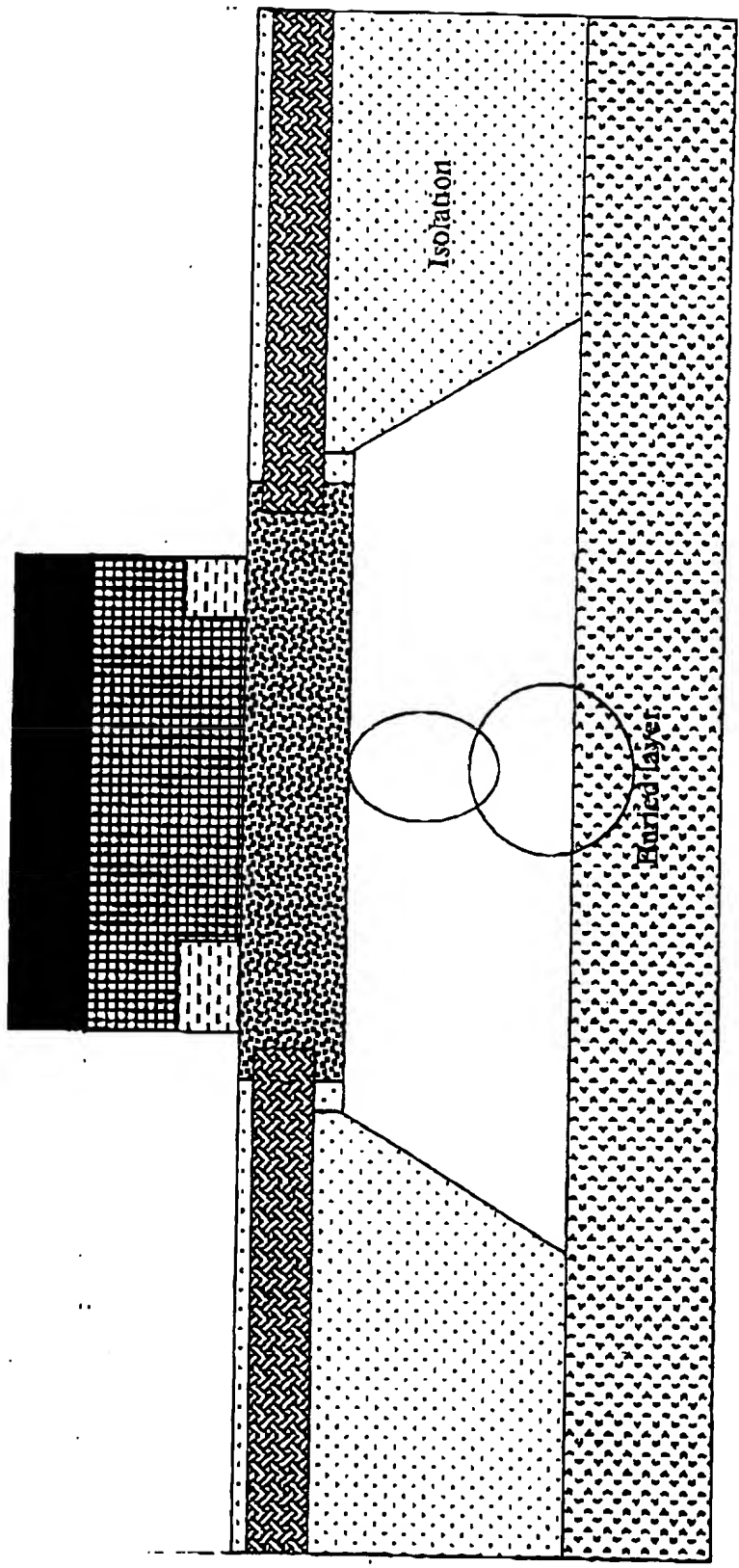
Process:

14. Emitter poly-Si deposition/doping

15. Emitter poly-Si patterning

H
g

14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100



- Process:
- 17 -16. Emitter poly-Si etch, nitride etch/stop on oxide
 - 14 -17. Extrinsic base implant

Fig 11